Applicant: Endres, et al.; Filing Date: 02/19/2004; For: Joint, Adaptive Control Of Equalization, Synchronization, And Gain In A Digital Communications Receiver

Atty. Docket No. S0465/283640; Express Mail # EV333523927US Sheet 1 of 13

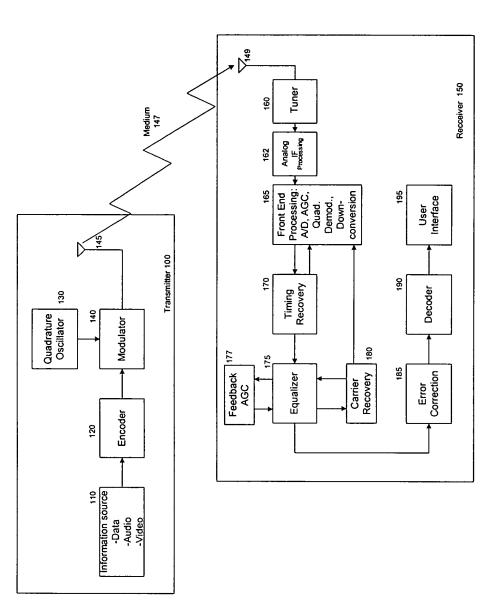


Figure 1: Typical prior-art communication system that may be employed for transmission of digital signals.

Applicant: Endres, et al.; Filing Date: 02/19/2004; For: Joint, Adaptive Control Of Equalization, Synchronization, And Gain In A Digital Communications Receiver
Atty. Docket No. S0465/283640; Express Mail # EV333523927US Sheet 2 of 13

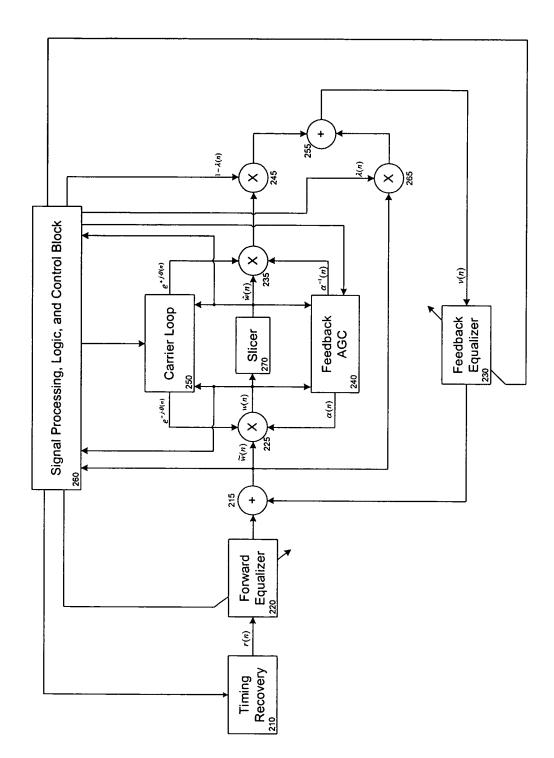


Figure 2: Block diagram of timing recovery, equalization, carrier recovery, and automatic gain control, jointly controlled by a central signal processing block in accordance with the present invention.

Applicant: Endres, et al.; Filing Date: 02/19/2004; For: Joint, Adaptive Control Of Equalization, Synchronization, And Gain In A Digital Communications Receiver Atty. Docket No. S0465/283640; Express Mail #

EV333523927US Sheet 3 of 13

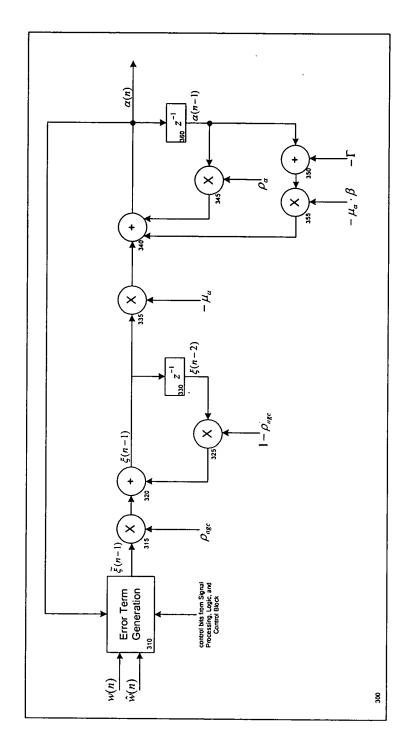


Figure 3: Diagram of preferred embodiment of Feedback AGC, showing adaptation of gain value at each symbol instance, and error term selection using control signals in accordance with the present invention.

Applicant: Endres, et al.; Filing Date: 02/19/2004; For: Joint, Adaptive Control Of Equalization, Synchronization, And Gain In A Digital Communications Receiver
Atty. Docket No. S0465/283640; Express Mail #
EV333523927US Sheet 4 of 13

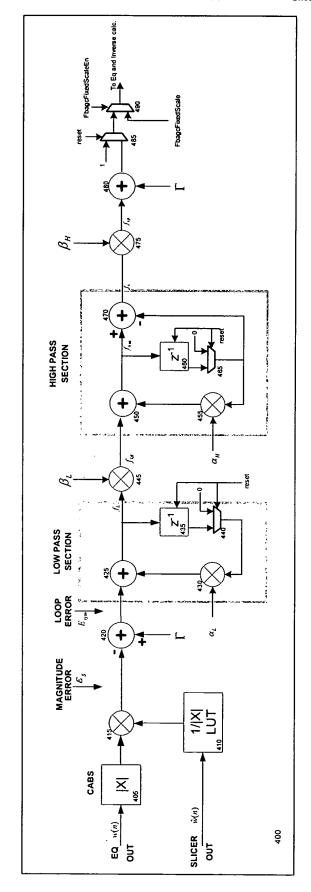


Figure 4: Diagram of alternative embodiment of Feedback AGC, showing error term generation, and bandpass filtering using cascaded low-pass and high-pass filter sections, in accordance with the present invention.

Applicant: Endres, et al.; Filing Date: 02/19/2004; For: Joint, Adaptive Control Of Equalization, Synchronization, And Gain In A Digital Communications Receiver
Atty. Docket No. S0465/283640; Express Mail # EV333523927US Sheet 5 of 13

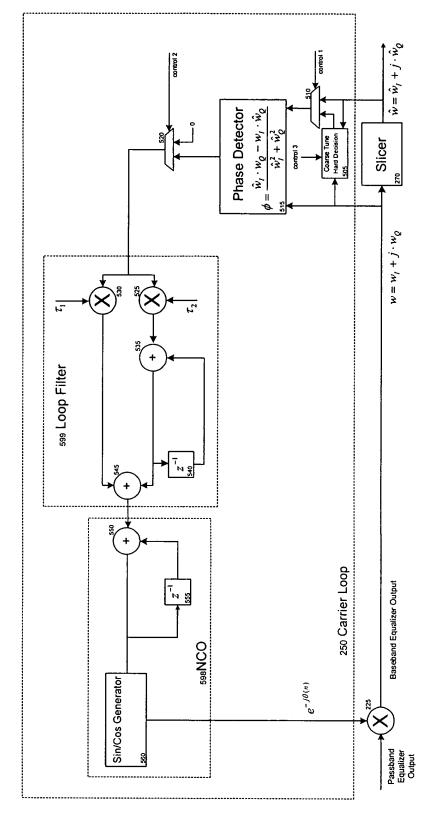


Figure 5: Diagram of Carrier Loop nested with Equalizer and Slicer, used to translate the received signal to precise baseband.

Applicant: Endres, et al.; Filing Date: 02/19/2004; For: Joint, Adaptive Control Of Equalization, Synchronization, And Gain In A Digital Communications Receiver
Atty. Docket No. S0465/283640; Express Mail # EV333523927US Sheet 6 of 13

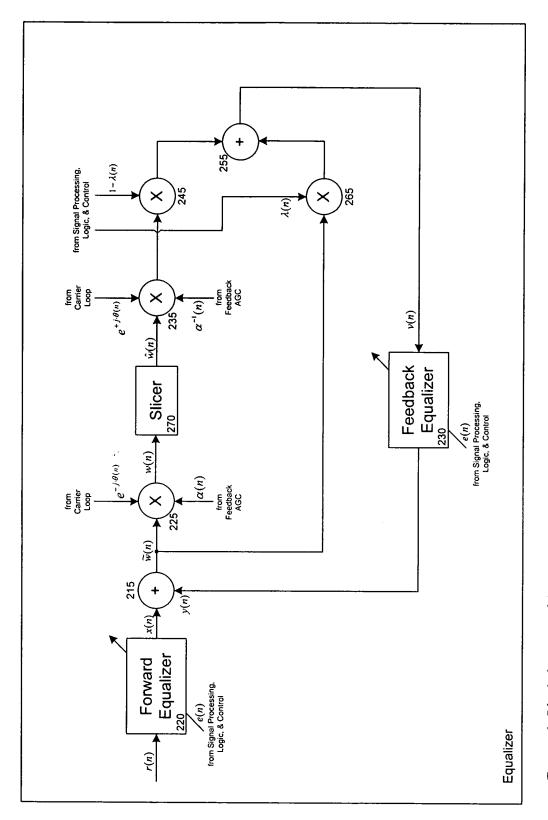


Figure 6: Block diagram of Decision Feedback Equalizer (DFE) in accordance with the present invention.

Applicant: Endres, et al.; Filing Date: 02/19/2004; For: Joint, Adaptive Control Of Equalization, Synchronization, And Gain In A Digital Communications Receiver

Atty. Docket No. S0465/283640; Express Mail # EV333523927US Sheet 7 of 13

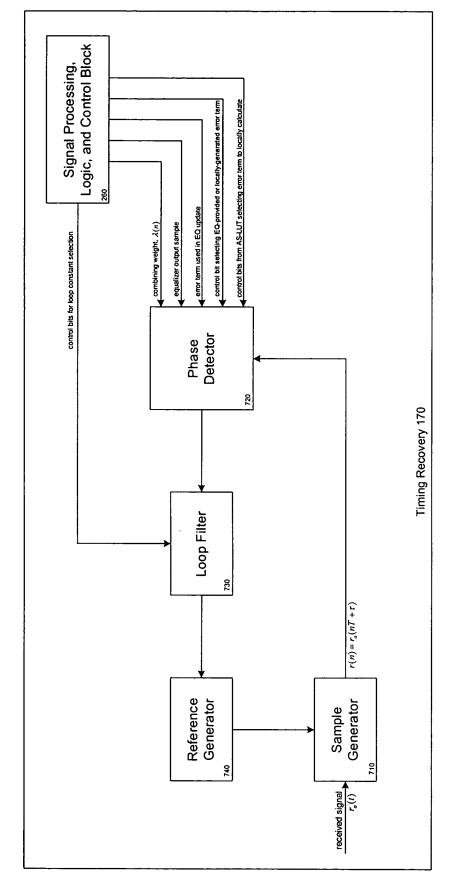


Figure 7: Block diagram of Timing Recovery Loop 170 and its control by Signal Processing, Logic, and Control Block 260 in accordance with the present invention.

Applicant: Endres, et al.; Filing Date: 02/19/2004; For: Joint, Adaptive Control Of Equalization, Synchronization, And Gain In A Digital Communications Receiver

Atty. Docket No. S0465/283640; Express Mail # EV333523927US Sheet 8 of 13

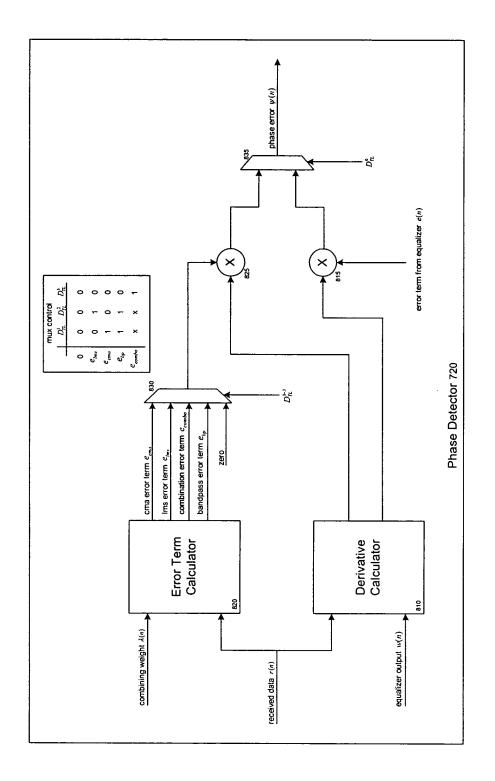


Figure 8: Phase Detector for Timing Recovery Loop and its control by the Signal Processing, Logic, and Control Block

Applicant: Endres, et al.; Filing Date: 02/19/2004; For: Joint, Adaptive Control Of Equalization, Synchronization, And Gain In A Digital

Communications Receiver
Atty. Docket No. S0465/283640; Express Mail # EV333523927US Sheet 9 of 13

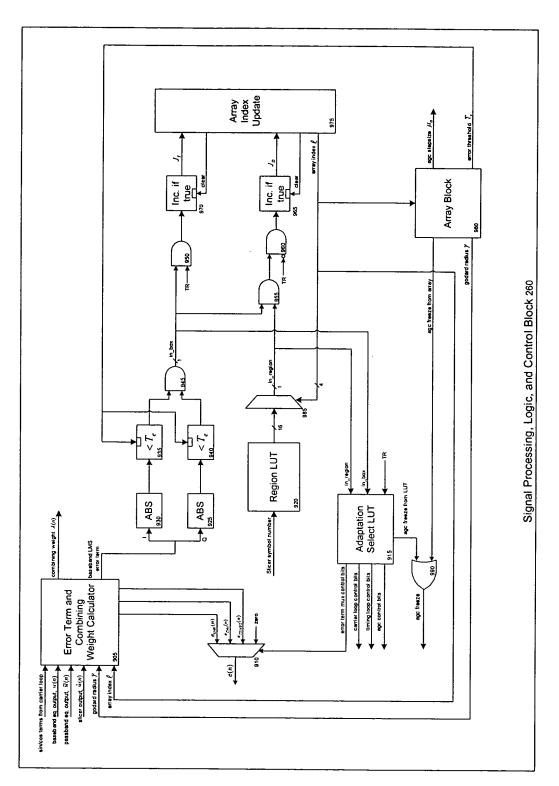


Figure 9: Signal Processing, Logic, and Control Block

Applicant: Endres, et al.; Filing Date: 02/19/2004; For: Joint, Adaptive Control Of Equalization, Synchronization, And Gain In A Digital Communications Receiver
Atty. Docket No. S0465/283640; Express Mail # EV333523927US Sheet 10 of 13

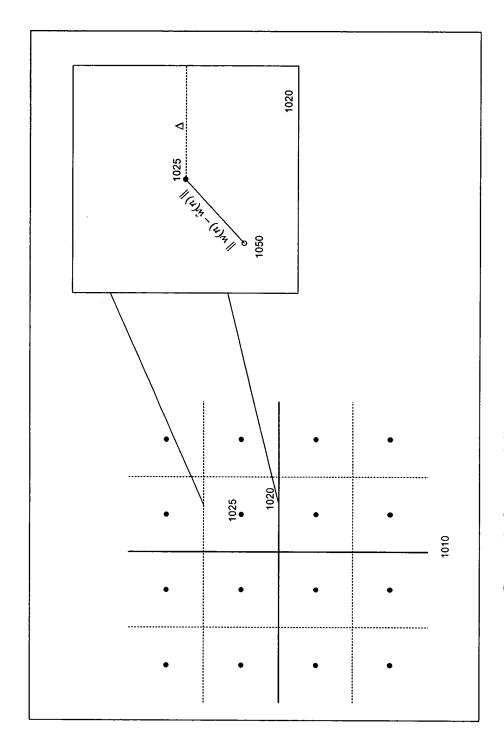


Figure 10: Conceptual illustration of combining weight calculation.

qApplicant: Endres, et al.; Filing Date: 02/19/2004; For: Joint, Adaptive Control Of Equalization, Synchronization, And Gain In A Digital Communications Receiver
Atty. Docket No. S0465/283640; Express Mail # EV333523927US Sheet 11 of 13

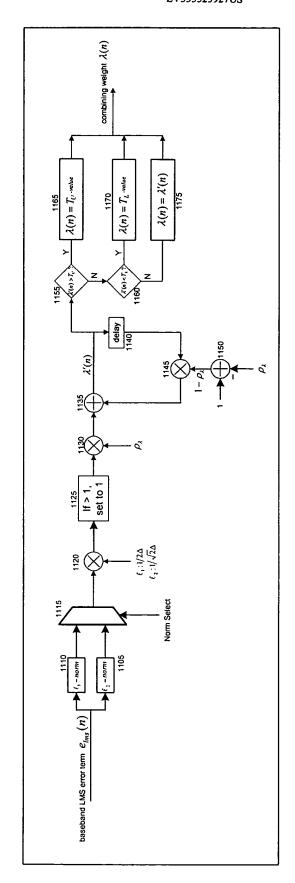
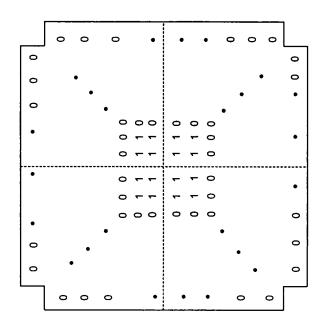


Figure 11: Circuit used to calculate combining weight $\lambda(n)$ in accordance with the present invention.

Applicant: Endres, et al.; Filing Date: 02/19/2004; For: Joint, Adaptive Control Of Equalization, Synchronization, And Gain In A Digital Communications Receiver
Atty. Docket No. S0465/283640; Express Mail # EV333523927US Sheet 12 of 13



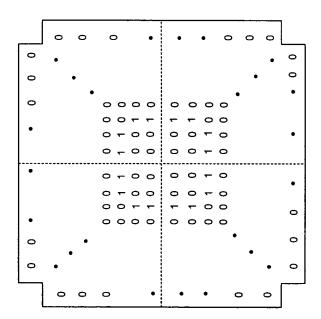


Figure 12: Conceptual drawing illustrating two possible templates used to discern a control signal in accordance with the present invention.

Applicant: Endres, et al.; Filing Date: 02/19/2004; For: Joint, Adaptive Control Of Equalization, Synchronization, And Gain In A Digital Communications Receiver

Atty. Docket No. S0465/283640: Express Mail #

Atty. Docket No. S0465/283640; Express Mail # EV333523927US Sheet 13 of 13

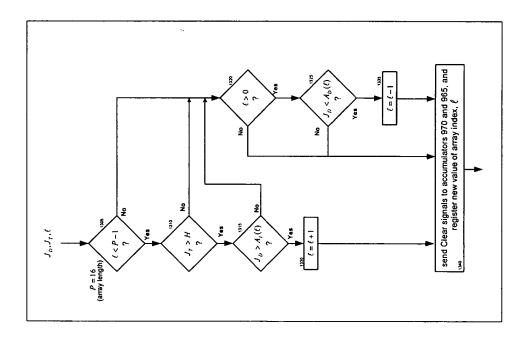


Figure 13:Flow diagram illustrating the update of array index ℓ in accordance with the present invention.